IN THE CLAIMS:

Please amend the claims as follows:

1-12. (Cancelled)

13. (Currently Amended) A memory buffer for a memory module board which is connected via a plurality of signal lines to a plurality of memory modules mounted on said memory module board having different signal line lengths, wherein the memory buffer comprises for each signal line a corresponding integration circuit for integrating the transmission time of a measurement pulse transmitted via said signal line between said memory buffer and a memory module connected to said signal line, and further wherein the memory buffer comprises a control logic which sends a measurement start command to the memory modules via a control line of a command and address bus.

14. (Cancelled)

15. (Previously Presented) The memory buffer according to claim 13, wherein the signal line is a data line of a bi-directional data bus.

16. (Cancelled)

17. (Previously Presented) The memory buffer according to claim 13, wherein the memory buffer comprises a measurement pulse detector which detects a measurement pulse received via said signal line.

18. (Previously Presented) The memory buffer according to claim 13, wherein the integration circuit of a signal line is connected to a corresponding measurement pulse detector of said signal line to receive a stop signal when a measurement pulse is detected by said pulse detector.

19. (Previously Presented) The memory buffer according to claim 13, wherein the memory buffer comprises a signal line delay memory for storing the integrated values of all integration circuits provided within said memory buffer as delay times of the corresponding signal lines.

20. (Currently Amended) The memory buffer according to claim 13, wherein the memory buffer ~~(1)~~ comprises a delay compensation unit which compensates the delay times of the signal lines depending on the delay times stored in said signal line delay memory to provide an equal standard time delay for all signal lines of said memory buffer.

21. (Previously Presented) The memory buffer according to claim 13, wherein the integration circuits are supplied with a phase adjusted clock signal generated by a clock phase generator to integrate time fractions of a clock period of a clock signal generated by a clock signal generator provided within said memory buffer.

22-23. (Cancelled)

24. (Previously Presented) The memory buffer according to claim 13, wherein the memory modules are DRAMs.

25. (New) A memory buffer for a memory module board which is connected via a plurality of signal lines to a plurality of memory modules mounted on said memory module board having different signal line lengths, wherein the memory buffer comprises for each signal line a corresponding integration circuit for integrating the transmission time of a measurement pulse transmitted via said signal line between said memory buffer and a memory module connected to said signal line, further wherein the memory buffer comprises a control logic which sends a measurement start command to the memory modules via a control line of a command and address bus, and further wherein each integration circuit is connected to the control logic to receive a start signal when the measurement start command is sent to the memory modules.

26. (New) A memory buffer for a memory module board which is connected via a plurality of signal lines to a plurality of memory modules mounted on said memory module board having different signal line lengths, wherein the memory buffer comprises for each signal line a corresponding integration circuit for integrating the transmission time of a measurement pulse transmitted via said signal line between said memory buffer and a memory module connected to said signal line, further wherein the memory buffer comprises a control logic which sends a measurement start command to the memory modules via a control line of a command and address bus, and further wherein the memory buffer comprises a measurement pulse

generator which transmits a measurement pulse via the signal line when the control logic sends a measurement start command to the memory modules.

27. (New) A memory buffer for a memory module board which is connected via a plurality of signal lines to a plurality of memory modules mounted on said memory module board having different signal line lengths, wherein the memory buffer comprises for each signal line a corresponding integration circuit for integrating the transmission time of a measurement pulse transmitted via said signal line between said memory buffer and a memory module connected to said signal line, further wherein the memory buffer comprises a delay compensation unit which compensates the delay times of the signal lines depending on the delay times stored in said signal line delay memory to provide an equal standard time delay for all signal lines of said memory buffer, and further wherein the delay compensation unit is connected via signal lines to a microcontroller mounted on a motherboard.